

1. A method for selecting an order in which to sift variables in a binary decision diagram comprising:-

traversing the graph in a depth first manner, thereby to produce a list of said labels in said selected order.

a processor adapted to arrange the said variables of said binary decision diagram in a representation of the nodes of a graph in which the nodes are labelled with the variables such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and to traverse the graph in a depth-first manner such that said processor outputs to said second store a list of said labels in said selected order.

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

using said selected order, controlling ~~sifting~~ each variable.

4. A method as claimed in claim 3 wherein said variables are sifted one-by-one to a deepest best location.

5. A method as claimed in claim 3 wherein said variables are sifted one-by-one in said selected order to a deepest best location followed by sifting in reverse order to a shallowest best location.

6. Apparatus for restructuring a binary decision diagram comprising:-

storage circuitry for storing bits representative of a set of functions as binary decision diagrams having a plurality of nodes labelled by variables;

a processor for detecting a number of nodes of said binary decision diagram, and in response to such detection, arranging the variables of said binary decision diagram on the nodes of a graph in which the nodes are labelled such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in a selected order and using said selected order, controlling sifting of variables of said binary decision diagrams;

wherein said sifted binary decision diagram is written by said processor to said storage circuits.

7. A method for proving the properties of a hardware system comprising:-

representing said system as binary decision diagrams having a plurality of nodes labelled by variables;

substituting functions which determine variables of internal signals;

arranging the variables of a binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponds to the set of functions which depend on the variables labelling the node; and

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traversing the graph in a depth-first manner to produce a list of said labels in a selected order;

using said selected order, controlling sifting each variable.

8. Apparatus for proving the properties of a hardware system comprising:

storage circuitry for storing bits representative of a set of functions which represent the hardware system as binary decision diagrams having a plurality of nodes labelled by variables;

a processor for substituting functions which determine the values of internal signals into the set of functions representing said system and detecting an increase in the number of nodes of said binary decision diagram, and, in response to such detection arranging the variable of said binary decision diagram on the nodes of a graph in which the nodes are labelled with the variables of the system such that the set of functions labelling leaves reachable from a node corresponding to the set of functions which depend on the variables labelling the node, traversing the graph in a depth-first fashion to produce a list of labels in said selected order, and using said selected order controlling sifting of the variables of said binary decision diagram; and

further comprising a second store, wherein said sifting binary decision diagram is written by said processor to said second store.

9. Apparatus as claimed in claim 8 wherein said number is a threshold derived from an original number of nodes.

10. Apparatus as claimed in claim 8 wherein said number of nodes is the number of nodes which branches on a predetermined variable.

11. Apparatus claimed in claim 8 wherein said number is an absolute number.

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